Unit 2.2: Alternative Design: Universal Gates and K Mapping

Content Area: **Science**
Course(s): **Digital Electro**
Time Period: **Semester 1**
Length: **3 weeks**
Status: **Published**

Standards

TEC.9-12.8.2.12.F.3	Select and utilize resources that have been modified by digital tools in the creation of a technological product or system (CNC equipment, CAD software).
TEC.9-12.8.2.12.G.1	Analyze the interactions among various technologies and collaborate to create a product or system demonstrating their interactivity. Technology is created through the application and appropriate use of technological resources.

Enduring Understandings

Understandings

Students will understand that …

1. There is a formal design process for translating a set of design specifications into a functional combinational logic circuit implemented with NAND or NOR gates.
2. Combinational logic designs implemented with NAND gates or NOR gates will typically require fewer Integrated Circuits (IC) than AOI equivalent implementations.
3. A NAND gate is considered a universal gate because it can be used to implement an AND gate, OR gate, and an INVERTER gate. Any combinational logic expression can be implemented using only NAND gates.
4. A NOR gate is considered a universal gate because it can be used to implement an AND gate, OR gate, and an INVERTER gate. Any combinational logic expression can be implemented using only NOR gates.
5. Karnaugh Mapping is a graphical technique for simplifying logic expressions containing two, three, and four variables.
6. A don't care condition is a situation where the design specifications "don't care" what the output is for one or more input conditions. Don't care conditions in K-Maps can lead to significantly simpler logic expressions and circuit implementations.

Essential Questions

Students will keep considering …

1. How can mathematical reasoning impact the design of a technological system?
2. How is the design of a technological system a trade-off between conflicting design demands and practical considerations?
3. Why are NAND gates and NOR gates considered universal gates and what are the advantages of implementing a combinational logic design with universal gates?

Knowledge and Skills

Knowledge

Students will …

1. Identify NAND and NOR gates and recognize them as universal gates.
2. Know that universal gates may provide the opportunity for a more efficient design.
3. Relate AOI logic to NAND only logic.
4. Relate AOI logic to NOR only logic.
5. Know the rules associated with the K-Mapping Technique.

Skills

Students will …

1. Translate a set of design specifications into a functional NAND or NOR combinational logic circuit following a formal design process.
2. Compare and contrast the quality of combinational logic designs implemented with AOI, NAND, and NOR logic gates.
3. Use Circuit Design Software (CDS) to simulate and prototype NAND and NOR logic circuits.
4. Use the K-Mapping technique to simplify combinational logic problems containing two, three, and four variables.
5. Solve K-Maps that contain one or more don't care conditions.
6. Use current technology to convert AOI designs to universal gate designs.

Resources

Technology Resources

- National Instruments Multiim circuit design and simulation software
- Microsoft Office Applications

Electronics Resources

- Electronics Trainers (power supply, function generator, breadboard)
- Electronics hand tools (diagonal cutters, needle-nosed pliers, wire strippers, etc.)
- Digital Multimeters
- Digital Transistor-Transistor Logic (TTL) integrated circuits
- TTL Chip Checker

Assessments

https://docs.google.com/document/d/1wR7bQF-8AQoRrt0g4C3hKja0yjwDjC9_BiAmONWbTcI/edit?usp=sharing

Modifications

https://docs.google.com/document/d/1ODqaPP69YkcFiyG72fIT8XsUIe3K1VSG7nxuc4CpCec/edit?usp=sharing